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09/778,233	02/06/2001	Lane Hauck	CYPR-CD00205.US.P	5757

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EXAMINER
CASIANO, ANGEL L

ART UNIT	PAPER NUMBER
2182	3

DATE MAILED: 08/07/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/778,233	Applicant(s) HAUCK ET AL.	
	Examiner Angel L. Casiano	Art Unit 2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 February 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 February 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The present Office Action is in response to application filed 06 February 2001.

2. Claims 1-27 are pending in the present application.

Drawings

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description:

- Fig. 1, "104"
- Fig. 6, "660"
- Fig. 7, "710" and "720"

A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

4. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "426" has been used to designate both "SO" pin and "CS#" pin (see Fig. 4). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

5. The disclosure is objected to because of the following informalities:

- Page 30, line 15; should read "Processor 800" instead of "Processor 810".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 6, 7 and 23 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

8. Claims 6 and 23 recite the limitation "said SPI device" in reference to claim 1 and claim 18, respectively. However, claim 1 (page 33, lines 18 and 25) and claim 18 (page 40, lines 14 and 21) recite a "first SPI device" and "second SPI device". It is unclear which SPI device "has a non-zero value located at its first address byte".

9. Claim 7 recites a "pulldown resistor weakly pulling down said D-IO pin..." This limitation is unclear, since the use of "weakly" results in confusion when interpreting the claim.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 1-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admission of prior art, in view of Gates [US 5,826,068].

Regarding claim 1, applicant admits to the prior art method including sending a "READ command" (see page 1, lines 26-27) from a memory controller (see page 1, line 13) chip to a serial peripheral interface (SPI) device (see page 1, lines 15-17) over an SPI interface (see page 1, line 10). In another aspect of the claim, Gates teaches a method of automatically detecting memory size (see col. 42, lines 17-22) and suggests a series of serial clock cycles, as part of the method (inherent, see col. 47, line 12; col. 48, lines 27-29). Nonetheless, the cited references do not teach automatically detecting the presence of non-zero values coming from the SPI device through a D-IO pin during a series of serial clock cycles. The cited art does not include an indication that the SPI device has memory addresses up to nine or sixteen bits, as claimed (see steps (d), (e)). However, it should be noted that Gates teaches a D-IO pin (see col. 47, lines 6-11) in a method of automatically detecting memory size. It would have been obvious for one of ordinary skill in the art at the time of the invention to combine teachings of Gates and applicant's knowledge to prior art because Gates' method, including a D-IO (bi-directional) pin, when incorporated into the admitted prior art, would have provided reduced cost and complexity as well as increased applicability (see Gates; col. 1, lines 46-54). Furthermore, although the cited art does not specify ("first", "second", "third", "fourth") serial clock cycles, the admission of prior art suggests these cycles (see page 1, lines 24-27; page 2, lines 1-5). Therefore, one of ordinary skill in the art at the time of the invention would have been motivated to modify the admitted method in order to include a bi-directional pin, as disclosed by Gates, in order to have

an improved automatic detection of memory sizes, since Gates teaches a method for these purposes.

As for claims 2 and 3, the cited art does not teach a first and second SPI device having up to 512 bytes (claim 2) and 64 kilobytes (claim 3) of memory, respectively. Nonetheless, Gates teaches detecting the memory size of an EEPROM (see col. 42, lines 17-22). Although Gates does not specifies 512 bytes or 64 kilobytes, it would have been obvious to one of ordinary skill in the art that the reference is capable of detecting different memory sizes (see col. 42, lines 17 and 22). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the invention that the claimed memory sizes constitute specific examples of the available EEPROM memory sizes. In addition, one of ordinary skill in the art at the time the invention was made would have been motivated to modify the admitted method, as exposed in the previous claim, by including a bi-directional pin (see Gates), in order to have an improved automatic detection of memory sizes, since Gates teaches a method for these purposes.

Considering claim 4, the cited art does not expressly teach a sensing circuit within a memory controller chip. Nonetheless, applicant admits to a memory controller (see page 1, line 13) chip in a method. In addition, Gates teaches a sensing circuit for automatically detecting memory size (see col. 41, line 10; Fig. 13, "1370"). It would have been obvious for one of ordinary skill in the art at the time the invention to combine teachings of Gates and applicant's knowledge to prior art because Gates' method, including a D-IO (bi-directional) pin, when incorporated into

admitted prior art methods, would have provided reduced cost and complexity as well as increased applicability (see Gates; col. 1, lines 46-54).

As for claim 5, applicant's admission of prior art includes a memory controller chip (see page 1, line 13) driving a serial clock signal (inherent, see page 2, lines 14-15) between a controller chip and an SPI device (see page 1, lines 13-17).

Considering claim 6, the prior art does not explicitly cite an SPI device having a non-zero value located at its first address byte. Nonetheless, Gates teaches detecting a non-zero value (see col. 42, lines 20-21) at a first memory address line, as part of a method for automatically detecting memory size of an SPI device (see "EEPROM", col. 42, line 22). Accordingly, one of ordinary skill in the art at the time the invention was made would have been motivated to combine the admitted prior art and the cited reference in order to provide reduced cost and complexity as well as increased applicability (see Gates; col. 1, lines 46-54) for a method of automatically detecting memory size.

As for claim 7, applicant admits to the prior art method including a memory controller (see page 1, line 13) chip and a serial peripheral interface (SPI) device (see page 1, lines 15-17) communicating over an SPI interface (see page 1, line 10). In addition, Gates teaches a method of automatically detecting memory size (see col. 42, lines 17-22) and suggests a series of serial clock cycles, as part of the method (inherent, see col. 47, line 12; col. 48, lines 27-29). The prior art disclosures do not specify the memory controller chip as having three controller pins.

Nevertheless, the admitted prior art teaches that the SPI interface (bus) is a "3-wire" interface (see page 2, lines 12-13, but taking into account all the necessary connections, it would be a "5-wire" interface (see page 3, line 5). It should be noted, however, that Gates teaches a D-IO pin ("bi-directional", see col. 47, lines 6-11) in a method of automatically detecting memory size. In another aspect of the claim, the prior art method does not explicitly include SI and SO pins coupled to a pulldown resistor. However, Gates teaches an SPI device having a resistor driving a pin to a logic "0" level (see col. 42, lines 7-9). It would have been obvious for one of ordinary skill in the art at the time of the invention to combine teachings of Gates and applicant's knowledge to prior art because Gates' method, including a D-IO (bi-directional) pin, when incorporated into prior art methods, would have provided reduced cost and complexity as well as increased applicability (see Gates; col. 1, lines 46-54) since it reduces the number of necessary pins. Therefore, one of ordinary skill in the art at the time of the invention would have been motivated to modify the admitted method in order to include a bi-directional pin, as disclosed by Gates, in order to have an improved automatic detection of memory sizes, since Gates teaches a method for these purposes.

As for claim 8, applicant's admission of prior art does not specify ("first", "second", "third", "fourth") serial clock cycles, but suggests these cycles (see page 1, lines 24-27; page 2, lines 1-5). Gates teaches a method of automatically detecting memory size (see col. 42, lines 17-22) and suggests a series of serial clock cycles (inherent, see col. 47, line 12; col. 48, lines 27-29). In addition, Gates teaches the indication of absence of an SPI device (see col. 42, line 5).

As for claim 9, Gates teaches a method of automatically detecting memory size (see col. 42, lines 17-22) and suggests a series of serial clock cycles, as part of the method (inherent, see col. 47, line 12; col. 48, lines 27-29). Nonetheless, the cited references do not explicitly teach automatically detecting the presence of zero or non-zero values coming from the SPI device through a D-IO pin during a series of serial clock cycles. The cited art does not include an indication that the SPI device has memory addresses up to twenty-four bits, as claimed. However, it should be noted that Gates teaches a D-IO pin (see col. 47, lines 6-11) in a method of automatically detecting memory size. It would have been obvious for one of ordinary skill in the art at the time the invention to combine teachings of Gates and applicant's knowledge to prior art because Gates' method, including a D-IO (bi-directional) pin, when incorporated into prior art methods, would have provided reduced cost and complexity as well as increased applicability (see Gates; col. 1, lines 46-54). Furthermore, although the cited art does not specify ("first", "second", "third", "fourth", "fifth") serial clock cycles, the admission of prior art suggests these cycles (see page 1, lines 24-27; page 2, lines 1-5). Therefore, one of ordinary skill in the art at the time of the invention would have been motivated to modify the admitted method in order to include a bi-directional pin, as disclosed by Gates, in order to have an improved automatic detection of memory sizes, since Gates teaches a method for these purposes.

As for claim 10, the prior art method does not explicitly include SI and SO pins coupled to a pulldown resistor. However, Gates teaches an SPI device having a resistor driving a pin to a logic "0" level (see col. 42, lines 7-9). It would have been obvious for one of ordinary skill in the art at the time the invention to combine teachings of Gates and applicant's knowledge to

prior art because Gates' method, including a D-IO (bi-directional) pin, when incorporated into prior art methods, would have provided reduced cost and complexity as well as increased applicability (see Gates; col. 1, lines 46-54) since it reduces the number of necessary pins. Therefore, one of ordinary skill in the art at the time of the invention would have been motivated to modify the admitted method in order to include a bi-directional pin, as disclosed by Gates, in order to have an improved automatic detection of memory sizes, since Gates teaches a method for these purposes.

As for claims 11-17, these constitute the SPI circuit for the method disclosed in claims 1-10. Claims 11-17 are therefore rejected under the same rationale.

As for claims 18-27, these are oriented to the system including instructions that when executed (see claim 18, liness26-27), implement the method disclosed in claims 1-10. Accordingly, the present claims are rejected under the same rationale.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

- Nizar et al. [US 2002/0010830 A1] teaches a method and apparatus for configuring memory devices.
- Stevens et al. [US 6,230,274 B1] discloses a method and apparatus for restoring a memory device channel when exiting a low power state.

- Nguyen et al. [US 6,055,600] teaches a method and apparatus for detecting and identifying the attributes of memory cache modules in a computer system.
- Lawrence et al. [US 5,995,424] teaches a memory test system.
- Gates et al. [US 5,920,708] teaches a host adapter integrated circuit containing data transfer modules having a serial port that uses a single serial port pin.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Angel L. Casiano whose telephone number is 703-305-8301. The examiner can normally be reached on 800-500pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey Gaffin can be reached on 703-308-3301. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7239 for regular communications and 703-746-7239 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

alc
August 4, 2003

JEFFREY GAFFIN
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